Docket No.: 204552016501
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yuichi SATO

Application No.: Not Yet Assigned
[Continuation of 09/412,328 filed October 5, 1999]

Art Unit: 2814

Filed: February 10, 2004

Examiner: Douglas A. Wille

For: STATIC RANDOM ACCESS MEMORY AND SEMICONDUCTOR DEVICE USING MOS TRANSISTORS HAVING CHANNEL REGION ELECTRICALLY CONNECTED WITH GATE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to 37 CFR §§1.97 and 1.98, Applicant submits for consideration in the above-identified application the documents listed on the attached Form PTO/SB/08. Copies of the documents were previously submitted in an Information Disclosure Statements and Office Actions, directed to the related application Serial Number 09/412,328, filed October 5, 1999, and, accordingly, copies are not included herewith. This protocol conforms with 37 CFR 1.98(d) and MPEP 609(A)(2). The Examiner is requested to make these documents of record in the application.

This Information Disclosure Statement is submitted with the application; accordingly, no fee or separate requirements are required.

Applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08, indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement under 37 CFR §§1.97 and 1.98 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the event that the transmittal form is separated from this document and the Patent Office determines that an extension and/or other relief (such as payment of a fee under 37 CFR 1.17 (p)) is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing 204552016501.

Dated: February 10, 2004

Respectfully submitted,

By: _____
Deborah S. Gladstein

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Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number 204552016501	Application Number NEW
Applicant: Yuichi SATO	
Filing Date February 10, 2004	Group Art Unit
Mailing Date February 10, 2004	

U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
	1.	7/1998	5,780,899	Hu et al.			
	2.	11/1998	5,831,899	Wang et al.			
	3.	9/1999	5,960,289	Tsui et al.			
	4.	2/2000	6,020,222	Wollesen			

FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES	Translation NO
	5.	3/1979	JP-A-54-037544	Japan			abs.	
	6.	8/1986	JP-A-61-185972	Japan			abs.	
	7.	1/1991	JP3022476	Japan			abs.	
	8.	2/1992	JP-A-04-053090	Japan			abs.	
	9.	6/1995	JP-A-07-161844	Japan			abs.	
	10.	5/1996	JP-A-07-176633	Japan			abs.	
	11.	8/1998	JP-A-10-222985	Japan			abs.	

OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title
	12.	*"PRINCIPLES OF CMOS VLSI DESIGN"*, A Systems Perspective, Second Edition, , Neil H.E. Weste and Kamran Eshraghian, Chapter 10, pp 578-83, 1992
	13.	F. Assaderaghi et al., "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI", IEEE Transactions on Electron Devices, vol. 44, no. 3, pp. 414-422, March 1997
	14.	Assaderaghi et al., 1994 "A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation" IEEE Electron Device Letters Vol. 15, pp 510-512.
	15.	Andoh et al., 1994 "Design methodology for low-voltage MOSFETS" IEEE International Electron Devices Meeting, Technical Digest, pp 79-82.
	16.	Assaderaghi et al., 1994 "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation" IEEE International Electron Devices Meeting, Technical Digest, pp 809-812.
	17.	David A. Hodges et al., "Analysis and design of digital integrated circuits", second edition, McGraw-Hill, Inc., PP 368-369; 1988

EXAMINER: | 1DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.